IN THE SPECIFICATION:

Please amend the Specification as follows.

Page 19, please amend the paragraph beginning on line 27 as follows:

FIG. 10 illustrates a first prior art configuration in which MAC 100 and PHY 120 communicate link partner capability to each other by way of microprocessor 110. Microprocessor management interface 104 is used to transfer link partner capability data 112 in LPCR 106 between flow control functions 102 of MAC 100 and microprocessor 110. In particular, the link partner PAUSE capability is used by MAC flow control functions 102 to enable the PAUSE function within MAC ~~102~~ 100. In turn, microprocessor 110 bidirectionally communicates with Serial Management Interface (SMI) controller 122. Controller 122 gets and puts the link capability data via LPRC 124, typically using a link partner capability signal 114, which may include IEEE-defined data signals MDIO and MDC. The serial management interface configuration generally is defined by the IEEE Standard 802.3. Autonegotiation controller 126 senses conditions on network channel 130, as well as input from another communication device, such as, for example, from another 10/100Base-T transceiver 140, having autonegotiation controller 142, therewithin.

Page 20, please amend the paragraph beginning on line 12 as follows:

FIG. 11 illustrates a second prior art configuration, this time in a microprocessorless environment. As before, MAC 200 and PHY 220 are not physically

integrated but reside on separate modules. SMI controller 210 and SMI controller 222 each include a state machine that facilitate the transfer of link partner capability data 216 and 218 between LPCR 204 in MAC 200 and LPCR 224 in PHY 220. Also, similar to FIG. 10, autonegotiation controller 226 senses conditions on network channel 230, as well as input from link partner 240, which, in this example, has autonegotiation controller 242, therewithin.

Page 20, please amend the paragraph beginning at line 22 to read as follows:

FIG. 12 is an implementation of the present invention that employs a single LPCR. Integrated 10/100Base-T communication device 301 is desired to be embodied as a monolithic VLSI component including MAC 302 and PHY ~~322~~ 321, most preferably in a single die configuration. Device 301 is capable of communicating data packets with a link partner according to a selectable communication protocol. This protocol may be a 10Base-T communication protocol or a 100Base-T communication protocol, and may be half- or full-duplex. Exemplary 100Base-T protocols include, without limitation, 100Base-T4, 100Base-TX, 100Base-FX, and 100Base-T2 communications protocols. Furthermore, device 301 is capable of functioning properly whether or not link partner 350 implements a flow control protocol, such as that defined by IEEE Standard 802.3x.